

FORM PTO - 1449 (Modified)

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S
INFORMATION DISCLOSURE STATEMENT

(Use several sheets if necessary)

Sheet 1 of 6

Application Number

10/790,966

Filing Date

March 2, 2004

First Named Inventor

Santosh P. Gaur et al

Group Art Unit

2131

Examiner Name

unknown

Attorney Docket Number

RPS920020014US1

UNITED STATES PATENT DOCUMENTS

Examiner Initials	Cite No.	Patent Document Number	Kind Code	Inventor	Date of Publication mm/dd/yyyy	Pages, Columns, Lines Where Relevant Passages Appear
/CK/	P1	4 817 140		Chandra et al.	03/28/1989	
/CK/	P2	5 088 033		Binkley et al.	02/11/1992	
/CK/	P3	5 247 577		Bailey et al.	09/21/1993	
/CK/	P4	5 430 850		Papadopoulos et al.	07/04/1995	
/CK/	P5	5 430 874		Kumazaki et al.	07/04/1995	
/CK/	P6	5 432 848		Butter et al.	07/11/1995	
/CK/	P7	5 446 906		Kardach et al.	08/29/1995	
/CK/	P8	5 619 660		Scheer et al.	04/08/1997	
/CK/	P9	5 663 896		Aucsmith	09/02/1997	
/CK/	P10	5 699 460		Kopet et al.	12/16/1997	
/CK/	P11	5 712 800		Aucsmith	01/27/1998	
/CK/	P12	5 719 436		Kuhn	02/17/1998	
/CK/	P13	5 724 027		Shipman et al.	03/03/1998	
/CK/	P14	5 757 919		Herbert et al.	05/26/1998	
/CK/	P15	5 793 101		Kuhn	08/11/1998	
/CK/	P16	5 818 939		Davis	10/06/1998	
/CK/	P17	5 822 255		Uchida	10/13/1998	
/CK/	P18	5 844 986		Davis	12/01/1998	
/CK/	P19	5 892 899		Aucsmith et al.	04/06/1999	

Examiner
Signature

/Cordelia Kane/

Date Considered

04/09/2007

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FORM PTO - 1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) Sheet 2 of 6	Application Number	10/790,966
	Filing Date	March 2, 2004
	First Named Inventor	Santosh P. Gaur et al
	Group Art Unit	2131
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/CK/	P20	5 930 483		Cummings et al.	07/27/1999	
/CK/	P21	5 937 063		Davis	08/10/1999	
/CK/	P22	5 940 591		Boyle et al.	08/17/1999	
/CK/	P23	5 941 987		Davis	08/24/1999	
/CK/	P24	5 949 881		Davis	09/07/1999	
/CK/	P25	5 968 176		Nessett et al.	10/19/1999	
/CK/	P26	5 991 797		Futral et al.	11/23/1999	
/CK/	P27	6 006 330		Soni	12/21/1999	
/CK/	P28	6 009 527		Traw et al.	12/28/1999	
/CK/	P29	6 011 910		Chau et al.	01/04/2000	
/CK/	P30	6 014 729		Lannan et al.	01/11/2000	
/CK/	P31	6 018 767		Fijolek et al.	01/25/2000	
/CK/	P32	6 021 201		Bakke et al.	02/01/2000	
/CK/	P33	6 026 085		Chau et al.	02/15/2000	
/CK/	P34	6 038 320		Miller	03/14/2000	
/CK/	P35	6 047 375		Easter et al.	04/04/2000	
/CK/	P36	2002/0099855		Bass et al.	07/25/2002	
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	First Named Inventor	Santosh Gaur et al
	Group Art Unit	2131
	Examiner Name	unknown
	Attorney Docket Number	RPS920020014US1

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Patent Document Number	Kind Code	Country	Date of Publication mm/dd/yyyy	Pages, Columns, Lines Where Relevant Passages Appear
/C.K./	F1	99/14881		WO	2/25/1999	
/CK/	F2	0 893 751		EP	01/27/1999	
/C.K./	F3	091 71500		JP	06/30/1997	
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	First Named Inventor	Santosh P. Gaur et al
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	Examiner Name	unknown
	Attorney Docket Number	RPS920020014US1

OTHER ART (Including Author (CAPITAL LETTERS), Title, Date, Pertinent Pages, etc.)		
Examiner Initials	Cite No.	
/CK/	N1	ALLEN Jr., J.R., et al., IBM PowerNP Network Processor: Hardware, software, and application, IBM Journal of Research & Development, March/May 2003, pp.177-193, Vol. 47, No. 2-3, IBM, USA.
/CK/	N2	AMERIJCKX C., et al., Architecture of a reconfigurable system based on an embedded FPPA, Proceedings of the SPIE - The International Society for Optical Engineering, 1998, pp. 141-149, Vol. 3526, SPIE- Int. Soc. Opt. Eng, USA.
/CK/	N3	BLEAKLEY C., et al., FILU-200 DSP coprocessor IP core, Conference Record of the Thirty-Third Asilomar Conference on Signals, Systems, and Computers (Cat. No. CH37020), 1999, pp. 757-761, Vol. 1, IEEE, Piscataway, NJ, USA.
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/CK/	N5	DAEMEN, J., et al., A Cryptographic Chip for ISDN and high speed multi-media applications, VLSI Signal Processing, VI (Cat. No.93TH0533-0), 1993, pp. 12-20, IEEE, New York, NY, USA.
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/CK/	N7	GAY C., Memory supervision with the M68000 processor. II. Realisation with the PMMU component, Elektronik, June 12,1987, pp. 94-96, 98, Vol. 36, No. 12, West Germany.
/CK/	N8	GORDON, DAVIS et al, U.S. Application 09/542,189, Network Processor with Multiple Instruction Threads, IBM Docket RAL920000008US1, filed April 4, 2000.
/CK/	N9	HERMANN K., et al., A programmable processing element dedicated as building block for a large area integrated multiprocessor system, 1996 proceedings. Eighth Annual IEEE International Conference on Innovative Systems in Silicon (Cat. No. 96CH35996), 1996, pp. 98-103, IEEE, USA.
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	Examiner Name	unknown
	Attorney Docket Number	RPS920020014US1

OTHER ART (Including Author (CAPITAL LETTERS), Title, Date, Pertinent Pages, etc.)		
Examiner Initials	Cite No.	
/CK/	N10	IYER, P., Intel Architecture Labs - Scalable Deployment of Ipsec in Corporate Intranets, Intel Architecture Labs Internet Building Blocks Initiative 2000, pp1-16
/CK/	N11	KONDO T., et al., Single-board SIMD processors using gate-array LSIs for parallel processing, IEICE Transactions on Electronics, December 1993, pp. 1827-1834, Vol. E76-C, No. 12, Japan.
/CK/	N12	LEISERSON, CE, et al., Communication-efficient parallel algorithms for distributed random-access machines, Algorithmica, 1988, pp. 53-77, Vol. 3, No. 1, West Germany.
/CK/	N13	LEMME, H., Are Chip Cards secure? Elektronik, August 1998, pp. 44-50, Vol. 47, No. 16, WEKA - Fachzeitschriften, Germany.
/CK/	N14	MANDL C., et al., Real-time search-processor architectures, Elektrotechnik und Informationstechnik, 1998, pp. 137-143, Vol. 115, No. 3, Springer-Verlag, Austria.
/CK/	N15	MCCAULEY, D.E., Shared Memory Model for a Dual-Processor File Server, IBM Technical Disclosure Bulletin, Vol. 34, No. 9, February 1992 pp. 336-337
/CK/	N16	MELEAR C, Floating point techniques using MC88000, WESCON/90 Conference Record, 1990, pp. 197-204, Los Angeles, CA, USA.
/CK/	N17	ROYO, A., et al., Design and implementation of a coprocessor for cryptography applications, Proceedings, European Design and Test Conference. ED & TC 97 (Cat. No. 97TB100102), pp. 213-217, IEEE Computer Soc. Press, Los Alamitos, CA, USA.
/CK/	N18	SANG WON LEE, et al., RAPTOR: a single chip multiprocessor, AP-ASIC'99. First IEEE Asia Pacific Conference on ASICs (Cat. No. 99EX360), 1999, pp. 217-220, IEEE, Piscataway, NJ, USA.
/CK/	N19	YEONG KANG LAI, An efficient array architecture with data-rings for 3-step hierarchical search block matching algorithm, Proceedings of 1997 IEEE International Symposium on Circuits and Systems. Circuits and Systems in the Information Age. ISCAS '97 (Cat. No. 97CH35987), 1997, pp. 1361-1364, Vol. 2, IEEE, New York, NY, USA.
Examiner Signature	/Cordelia Kane/	
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/CK/	N20	High Speed Serial Interface Micro Channel Adapter, IBM TDB, Vol 34, No. 7A, December 1991, pp299-301
/CK/	N21	Developing Embedded System Control Programs, IBM TDB, Vol. 39, No. 10, October 1996, pp151-152
/CK/	N22	Task Switching Between Processing Using the Sequencer, IBM TDB, Vol 35, No. 7, December 1992, pp362-363
/CK/	N23	HIPP III 8300 FlowThrough Security Processor, Hifn Intelligent Secure Netorking
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